Table 4: RENA-2 Specifications. Some items refer to Table 1 and other figures.

No.	Specification	Conditions	Min	Typ	Max	Comments
1	Full scale signal range	Range A, see Table 1	9 fC (250 keV for CZT)			Selection on a channel-by-channel basis of one of two full scale signal ranges. This minimum FSR must be achieved in all good parts, despite absolute capacitance tolerance for fabrication process.
2	Full scale signal range	Range B, see Table 1	54 fC (1.5 MeV for CZT)			
3	Allowable DC input current	Positive polarity, see Table 1	-100 pA		5 nA	Small reverse input currents can occur in AC coupled systems, due to protection diode or coupling capacitor leakage.
4		Negative polarity, see Table 1	-5 nA		100 pA	
5	σ_{inp} (total rms noise and error, input referred)	Range A, Cap-opt A, C_d = 2 pF, see Table 1			18 aC	This is equivalent to 112 electrons, a dynamic range of 500.
6		Range A, Cap-opt B, C_d = 9 pF, see Table 1			18 aC	
7		Range B, Cap-opt A, C_d = 2 pF, see Table 1			54 aC	This is equivalent to 337 electrons, a dynamic range of 1000.
8		Range B, Cap-opt B, C_d = 9 pF, see Table 1			54 aC	

Table 4: *Continued*

No.	Specification	Conditions	Min	Typ	Max	Comments
9	$\partial\sigma_{inp} / \partial C_d$	Range A, Cap-opt A, C_d = 2 pF, see Table 1		TBD		Selectable (on a channel-by-channel basis) noise optimization by changing the input transistor width using a control bit. Optimized for two capacitance input values.
10		Range A, Cap-opt B, C_d = 9 pF, see Table 1		TBD		
11		Range B, Cap-opt A, C_d = 2 pF, see Table 1		TBD		
12		Range B, Cap-opt B, C_d = 9 pF, see Table 1		TBD		
13	Minimum operating trigger threshold requirement (applies to all channels simultaneously)	Range A, see Table 1			100 aC	This is equivalent to 624 electrons.
14		Range B, see Table 1			580 aC	This is equivalent to 3620 electrons.
15	Test signal coupling capacitance			75 fF		This implies that a 707 mV step will inject the full scale (range B) signal of 53 fC
16	Number of active channels		36			In addition, a dummy channel for matching is at each end of array.
17	Peaking time constant	16 selections 0-15	0.36, 0.39, 0.41, 0.45, 0.49, 0.54, 0.59, 0.66, 0.91, 1.08, 1.27, 1.69, 1.82, 2.80, 4.46, 38.0 μs nominal			16 selections available on a channel by channel basis
18	Power dissipation	Event rate 1 kHz, single hits		6mW	TBD	Goal is 5 mW/ch, estimate 6 mW/ch with fast trigger path disabled. Channel power down available on a per channel basis. Off channels dissipate < 0.5mW each.

Table 4: *Continued*

No.	Specification		Conditions	Min	Typ	Max	Comments
19	Total dose (γ) tolerance		<50% failure	20 kRad(Si)			SEU is not a concern. The radiation specs are goals to be attempted on a best effort basis with standard CMOS technology, no special process.
20	Destructive SEL		TBD			0	
21	Timing jitter		See Table 1			10 ns (or better)	Note that this is for input pulses of fixed amplitude - it excludes time walk due to amplitude variation.
22	Discriminator threshold DAC number of bits			8			
23	Discriminator threshold DAC DNL			1 bit, guaranteed monotonic			
24	Discriminator threshold DAC range			Determined by external voltage input, settable from 0 up to FS signal range			
25	Synchronous CMOS	Cycle time requirement		30 ns			Typical application system will use a direct connection to Xilinx Spartan-series FPGA (or similar) running at 32 MHz.
26		Setup time requirement		12 ns			
27		Hold time requirement		0 ns			
28		Data valid time		10 ns			

Table 4: *Continued*

No.	Specification	Conditions	Min	Typ	Max	Comments
29	EMI-critical signal standards		LVDS or low-swing (150 mV) version			Applies only to TRIG, RST, and ACQUIRE signals (all asynchronous)
30	Analog output architecture		Differential out with disable, to drive capacitive load only; 4 or more RENA 2000 bussed together to single A/D			
31	Analog output settling time	C_L = TBD, 12-bit settling			TBD	Goal is 333 ns
32	Analog output format		For each channel marked in the read register, peak detector level and (if enabled) U and V timestamp levels			
33	Dead time per event	Event with n channels to read; HIT/READ register is read and written	TBD	TBD	TBD	Goal is 5 μs + n*(333 ns)
34	Input pad pitch		125 μm			